

Design and Analysis of a New Power Efficient Half Subtractor at Various Technologies

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ABSTRACT: Three designs of half subtractor in this paper, one is TL second is PTL design and third is proposed. These designs are implemented on two technologies 90 nm and 45 nm using tanner eda. Power consumption is calculated on various supply voltages and. Results are prepared by comparisons between all the three designs and our results for proposed half subtractor are found satisfactory.

KEYWORDS: TL, PTL, Average power, Half subtractor.

I. INTRODUCTION

A conventional Half-subtractor circuit is a combinational circuit that can be used to subtract one binary digit from another to produce a Difference output and a Borrow output. Functionally, the half subtractor consists of a 2 input XOR Gate, an INVERTER and a 2 input AND gate. The Borrow output here specifies whether a „1“ has been borrowed to perform the subtraction. The Half-Subtractor at the gate-level and truth table are shown in Fig 1.1 and Table 1.1.

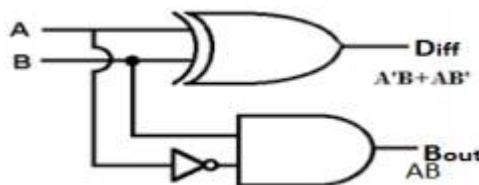


Fig.1: Gate Level 1 bit Half Subtractor.

Table 1 Truth Table of 1 bit half subtractor.

A	B	B _{out}	Diff
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

The Boolean expression for the two output variables are given by the equations.

$$\text{Diff} = A'B + AB'$$

II. RESULT

The Below figure shows the designed TL half subtractor.

TL half subtractor:

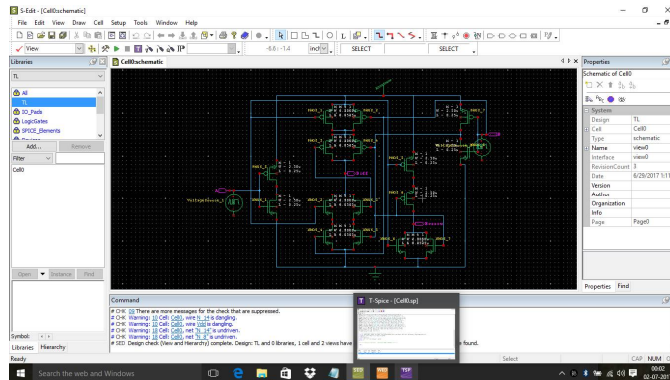


Figure 1: TL half subtractor

The figure 1 shows the TL half subtractor.

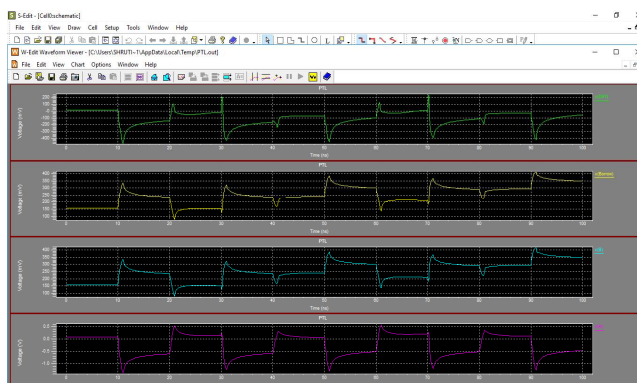


Figure 2: TL half subtractor waveform

The figure 2 shows the waveform of TL half subtractor.

Parameters calculated for TL half subtractor:

Below table shows the average power calculated for various voltages.

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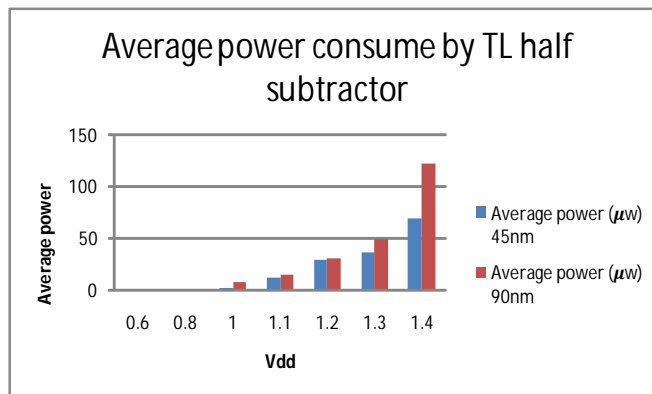
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Table 2: Average power consumed of TL half subtractor

Vdd(V)	Average power (μ w)	
	45nm	90nm
0.6	0.0040	0.041
0.8	0.074	0.758
1.0	2.09	8.049
1.1	11.28	18.76
1.2	27.91	35.99
1.3	35.59	60.01
1.4	68.07	90.95



Graph 1: Vdd vs Average power of TL

The above graph shows that average power consumes by TL half subtractor at 45 nm consume lesser then 90nm.

PTL half subtractor:

Figure 3 shows PTL half subtractor circuitry design.

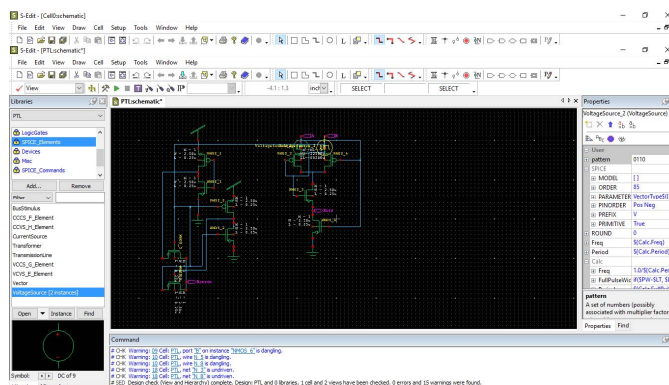


Figure 3: PTL half subtractor

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Figure 4 shows the waveform of PTL half subtractor.

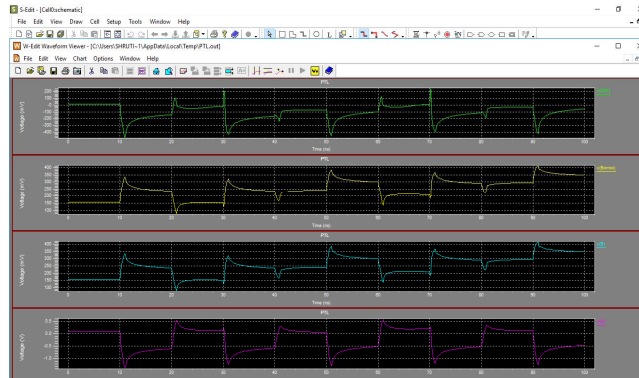


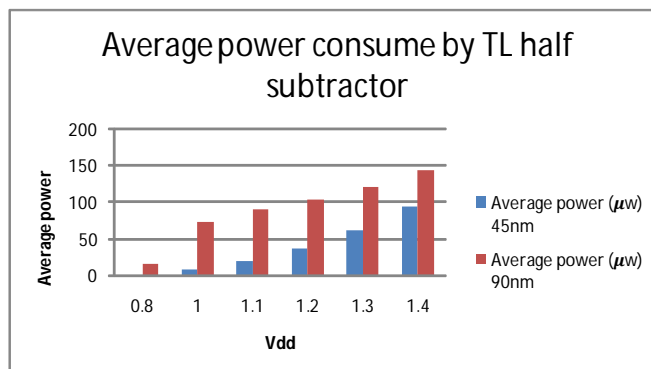
Figure 4: PTL half subtractor waveform

Parameters calculated for PTL half subtractor:

Below table shows the average power calculated for various voltages.

Table 3: Average power consumed of PTL half subtractor

Vdd(V)	Average power (μ w)	
	45nm	90nm
0.8	0.98	14.53
1.0	8.68	73.32
1.1	19.79	89.39
1.2	37.34	103.78
1.3	61.59	119.89
1.4	93.48	143.47



Graph 2: Vdd vs Average power of PTL

The above graph shows that average power consumes by PTL half subtractor at 45 nm consume lesser then 90nm.

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Proposed half subtractor:

Figure 5 shows the proposed half subtractor.

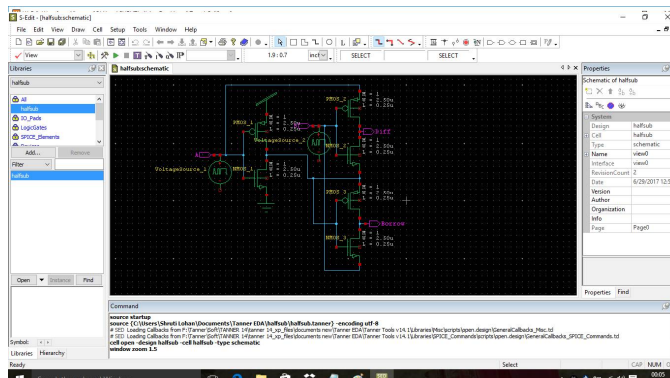


Figure 5: Proposed half subtractor

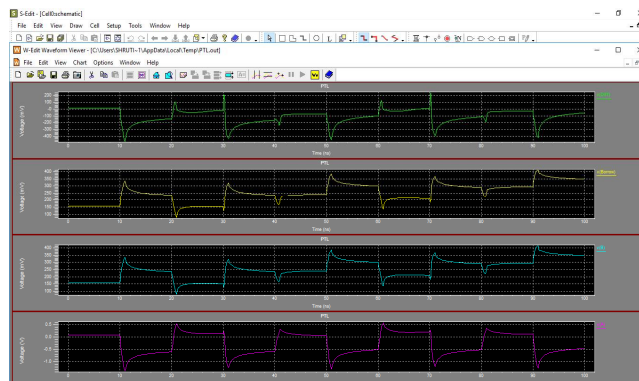


Figure 6: Proposed half subtractor waveform

The above figure shows the waveform of the proposed half subtractor.

Parameters calculated for proposed half subtractor:

Below table shows the average power calculated for various voltages.

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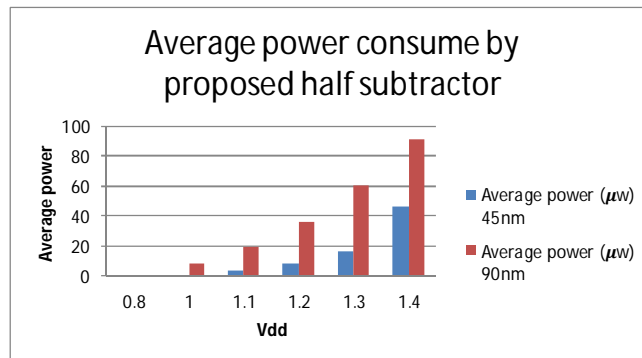
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Table 4: Average power consumption at various voltages at 45nm and 90 nm technology

Vdd(V)	Average power (μw)	
	45nm	90nm
0.8	0.099	0.041
1	0.150	0.72
1.1	2.96	6.74
1.2	7.73	14.87
1.3	16.59	29.68
1.4	46.07	49.01



Graph 3: Vdd vs Average power of Proposed HS at 45nm and 90nm

The above graph shows that average power consumes by proposed half subtractor at 45 nm consume lesser then 90nm

III. COMPARISON BETWEEN PROPOSED, AND PTL HALF SUBTRACTOR

At 45nm

Comparison between proposed, TL and PTL at 45nm at various Vdd is done below with the help of table. Below table shows the average power calculated for various voltages.

Table 5 : Average power consumed at various Vdd by proposed ,TL and PTL half subtractor at 45nm

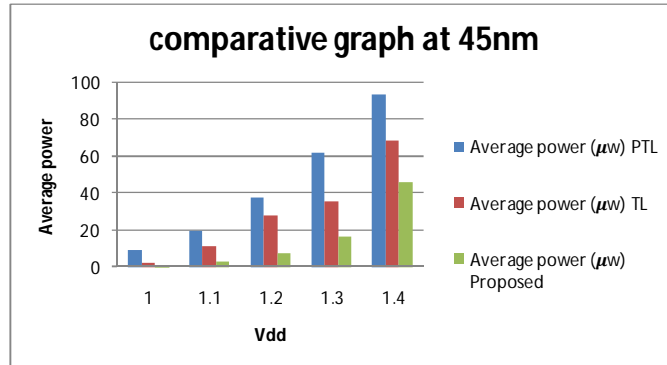
Vdd(V)	Average power (μw)		
	PTL	TL	Proposed
0.8	0.98	0.41	0.099
1.0	8.68	0.72	0.150
1.1	19.79	6.74	2.96
1.2	37.34	14.87	7.73
1.3	61.59	29.68	16.59
1.4	93.48	49.01	46.07

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Graph 4: Vdd vs Average power of Proposed HS at 45nm

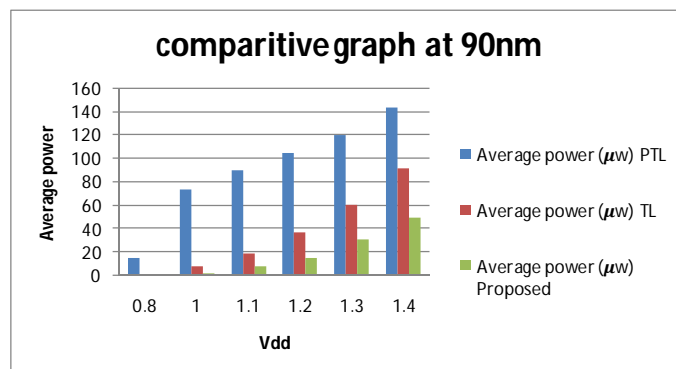
The above graph shows that average power consumes by proposed half subtractor at 45 nm is lesser and PTL consume high average power.

At 90nm

Comparison between proposed, TL and PTL at 90nm at various Vdd is done below with the help of table. Below table shows the average power calculated for various voltages.

Table 6: Average power consumed at various Vdd by proposed ,TL and PTL half subtractor at 90nm

Vdd(V)	Average power (µw)		
	PTL	TL	Proposed
0.8	14.53	0.758	0.041
1.0	73.32	8.049	0.72
1.1	89.39	18.76	6.74
1.2	103.78	35.99	14.87
1.3	119.89	60.01	29.68
1.4	143.47	90.95	49.01



Graph 5: Vdd vs Average power of Proposed HS at 90nm

The above graph shows that average power consumes by proposed half subtractor at 90 nm is lesser and PTL consume high average power.

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IV. CONCLUSION

After comparison of TL, PTL and proposed half subtractor at 90nm on various voltages it is concluded that proposed half subtractor consumes low average power. So, further work is done on 90nm technology .

Comparison between 90nm and 45nm technologies at various Vdd is done. It can be seen that on increasing Vdd power consumption is also increased. Vdd is varied from 0.8v to 1.4v and maximum power consumption by PTL is 143.47 μ w ,TL is 90.95 μ w and proposed is 49.01 μ w on 90 nm technology and minimum power consumption is 14.53 by PTL,0.78 by TL and 0.041 by proposed on 90nm technology

Maximum power consumption by PTL is 93.98 μ w ,TL is 49.01 μ w and proposed is 46.01 μ w on 45 nm technology and minimum power consumption is 0.98 by PTL,0.41 by TL and 0.099 by proposed on 45nm technology

The proposed half subtractor offered less power consumption on both technologies.

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